Claims:

1. A computer system, comprising:

a first processor;

a second processor; and

a direct memory access (DMA) engine capable of being executed by one of the first and second processors, the DMA engine capable of transferring data between one or more resources in the computer system.

2. The system of Claim 1, wherein the direct memory access engine further comprises one or more instructions being executed by one of the first and second processors that transfer data between the resources.

3. The system of Claim 2, wherein the resources comprise one or more of static random access memory, dynamic random access memory and one or more hardware buffers that are capable of interfacing with one or more peripheral devices.

4. The system of Claim 3, wherein the one or more hardware buffers, in combination with the DMA engine, permit the one or more peripherals to access the memory directly.

5. The system of Claim 3, wherein the instructions further comprise a store multiple data instruction and a load multiple data instruction wherein the load multiple data instruction loads data from multiple locations in one of the hardware buffers into multiple locations in the internal registers in the processor executing the DMA engine instructions and wherein the store multiple data instruction transfers the data from multiple locations in the internal registers into multiple locations in a memory.

6. A computer implemented direct memory access apparatus that operates in a computer system having two or more processors, the apparatus comprising:

a load multiple data instruction capable of being executed by a processor in the computer system for loading data from multiple locations in a resource into multiple locations in an internal register in the processor; and

a store multiple data instruction capable of being executed by the processor in the computer system for storing data from multiple locations in the internal registers in the processor into multiple locations in a memory.

7. The apparatus of Claim 6, wherein the resources comprise one or more of static random access memory, dynamic random access memory and one or more hardware buffers that are capable of interfacing with one or more peripheral devices.

8. The apparatus of Claim 7, wherein the one or more hardware buffers, in combination with the DMA engine, permit the one or more peripherals to access the memory directly.

9. The apparatus of Claim 8, wherein the instructions further comprise a store multiple data instruction and a load multiple data instruction wherein the load multiple data instruction loads data from multiple locations in one of the hardware buffers into multiple locations in the internal registers in the processor executing the DMA engine instructions and wherein the store multiple data instruction transfers the data from multiple locations in the internal registers into multiple locations in a memory.

10. A computer implemented direct memory access apparatus that operates in a computer system having two or more processors, the apparatus comprising:

a load multiple data instruction capable of being executed by a processor in the computer system for loading data from multiple locations in a resource into multiple locations in an internal register in the processor; and

a store multiple data instruction capable of being executed by the processor in the computer system for storing data from multiple locations in the internal registers in the processor into multiple locations in a memory; and

a data buffer FIFO capable of accepting multiple data transfers to and from any of its alias addresses.